Semiconductor Glossary

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Term (Index)	Definition
CD	critical dimension; term related to the geometry of features of an integrated circuit.

Term (Index)	Definition
critical dimension, CD	dimensions of the smallest geometrical features (width of interconnect line, contacts, trenches, etc.) which can be formed during semiconductor device/circuit manufacturing using given technology.

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abbreviation is written with a subscript lowercase letter.)

Cpk — see process capability index. (The "pk" part of the abbreviation is written with subscript lowercase letters.)

crack *n* — 1 : *on semiconductor wafers*, a cleavage or fracture that extends to the surface and may or may not pass through the entire thickness of the wafer. [ASTM F1241] 2 : *of a semiconductor package or solder preform*, a cleavage or fracture that extends to the surface. The crack may or may not pass through the entire thickness of the package or preform. [SEMI G61-94] 3 : *in flat panel display substrates*, a fissure located at the sheet edge or central area. [SEMI D9-94]

cracked bead *n* — *in an ion-exchange resin*, a bead (of an ion-exchange resin material) that exhibits a visible crack when viewed at 20X magnification. [SEMATECH]

crater *n* — *on the surface of a slice or wafer*, an individually distinguishable bowl-shaped cavity. A crater is visible when viewed under diffused illumination. [SEMATECH]

cratering *n* — *on a slice or wafer*, a surface texture of irregular closed ridges with smooth central regions. [ASTM F1241]

creep *n* — 1 : a measurement of the seating action of a regulator, determined by the increase in outlet pressure when flow is decreased from almost zero (0.1% of the maximum rated flow) to zero. 2 : the gradual change in dimensions of an object from prolonged exposure to high temperature or stress. [SEMATECH]

crescents *n* — structures with parallel major axes, attributed to substrate defects either above or below the surface plane of silicon substrates after epitaxial deposition. [ASTM F1241] Also see fishtails.

criterion-referenced instruction *n* — a way of organizing and managing instruction in which prespecified performance criteria are achieved by each qualified learner. Also called *mastery learning*.

critical area *n* — the area in which the center of a defect must occur to cause a failure or fault. [SEMATECH] Also see fault and fault probability.

critical dimension — the width of a patterned line or the distance between

(CD) *n*	two lines, monitored to maintain device performance consistency; that dimension of a specified geometry that must be within design tolerances. [ASTM F127-84] Also see linewidth.
critical path *n*	*in a project*, the longest sequence of interdependent activities. The delay of any critical path activity will cause a corresponding delay in completion of the project. [SEMATECH]
critical pressure *n*	the pressure at which a substance may exist as a ga in equilibrium with the liquid at the critical temperature [SEMI Chemicals/Gases, Vol. 1, 1990 (no longer in print)]
critical seal area *n*	*on a semiconductor package*, the area bounded by the shortest distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area. [SEMI G1-85] Contrast noncritical seal area. Also see critical seal path.
critical seal path *n*	*on a semiconductor package*, the shortest nominal design distance from the edge of the largest cavity, usually the wire bond cavity, to the edge of the edge of the package or the minimum width of the ceramic layer forming the seal area. [SEMI G61-94] Also see critical seal area. Contrast seal area.
critical temperature *n*	the temperature above which gas cannot be liquefiec by pressure alone. [SEMI Chemicals/Gases, Vol. 1, 1990 (no longer in print)]
CRM *n*	see cost/resource model.
crossbar *n*	the structure that connects the two sides of a wafer carrier at the bar end of the carrier and is used to align the carrier to processing equipment. [SEMATECH] Also called a *bar* or an *H-bar*.
crossbow *n*	the transverse bowing of a leadframe strip. [SEMI G! 89] Contrast coil set. Also see package.
crosscut technologies *n*	in the categorization of technologies, specific technologies that are required by several of the primary technologies identified in the National Technology Roadmap for Semiconductors. For example, metrology is a common need of all the Roadmap's primary technologies required for integrated circuits, thus metrology is a crosscut technology. [1994 National Technology Roadmap for Semiconductors]

keypad, and many stations include host computer interfacing capabilities for processing and storing this data.[65]

In more automated systems, the human operator is completely removed from the defect inspection task. *In-process wafer inspection systems*, based on automatic image processing have been introduced. Defect detection is accomplished either by die-to-die or die-to-database comparison. Manufacturers of these systems claim defect detection sensitivities well into the sub-micron range. Such instruments, however, often have difficulty detecting particles on substrates that have surface granularity, or particles on wafers containing surface topography. In addition, for particles near the minimum-size detection limit, such machines can miss the presence of some particles, and signal the detection of others that may be non-existent.

The remainder of this section discusses linewidth measurement techniques used to verify that critical dimensions have been produced. Procedures are described for monitoring the variation of linewidths produced in a production environment as a function of time. Such data can serve as a gauge for tracking the performance of a lithographic process line.

12.4.7.1 Linewidth Variation and Control. There are two aspects of feature sizes that must be controlled in the lithographic/etching process: 1) the absolute size of a minimum feature, including linewidth, spacing, or contact dimensions (also referred to as a *critical dimension*, or CD), and 2) the variations of the minimum feature sizes as they cross steps on wafer surfaces. Linewidth (and spacing) measurements are regularly performed to determine the actual sizes of CDs at each masking level of a process. The variation of linewidths over steps are also monitored (causes of the variation were discussed in the section on *Resist Processing: Exposure*). These two aspects are mentioned together because a tradeoff exists between absolute linewidth size and variation of the size over steps. Over-exposure and over-development can improve linewidth control, but at the expense of linewidth size. Figure 12-36 shows a SAMPLE simulation which calculates linewidth variation ΔL across a 0.5 μm step, as the line sizes vary with changing exposure and development. It shows that linewidth variation over steps can be considerably reduced by over-exposure, but at the expense of dimensional accuracy.[64]

Another issue involving linewidth control is that correct feature *sizes* must be maintained across an entire wafer, and from one wafer to another. The ability to do this is referred to as *linewidth control*. As feature size is reduced, the tolerable error on feature size control is also

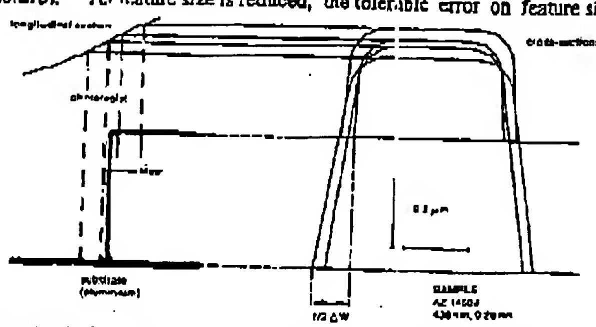

Fig. 12-36 Longitudinal section and cross sections of a photoresist line running across a one micron aluminum step. The resist profiles are simulated by SAMPLE. The nominal linewidth is 1.8 μm.[64] Reprinted with permission of SPIE.